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1 A multi-interval Chebyshev collocation method for efficient high-accuracy RF circuit simulation

Baolin Yang, Joel Phillips

June 2000 **Proceedings of the 37th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(138.88 KB) Additional Information: full citation, abstract, references, citings, index terms

Most RF circuit analysis tools use either shooting-Newton or harmonic balance methods. Neither can efficiently achieve high accuracy on strongly nonlinear circuits possessing waveforms with rapid transitions. We present a multi-interval-Chebyshev (MIC) method that discretizes the circuit equations by dividing the simulation domain into a set of intervals whose size is adaptively chosen and using Chebyshev polynomials to represent the solution in each interval. The MIC method has excellent s ...

2 A local circuit topology for inductive parasitics

Andrea Pacelli

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Publisher: ACM Press

Full text available: pdf(220.01 KB) Additional Information: full citation, abstract, references, citings, index terms

A novel circuit topology for inductive coupling between interconnecting wires is presented. The model is local, i.e., only coupling between neighboring wires is explicitly modeled. However, the topology accounts for long-range coupling by propagating the vector potential from one wire to the next. Examples of model calibration, both directly from layout and as model-order reduction of a given inductance matrix, are presented for simple wiring structures.

3 CAD for RF circuits

P. Wambacq, G. Vandersteen, J. Phillips, J. Roychowdhury, W. Eberle, B. Yang, D. Long, A. Demir

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: IEEE Press

Full text available: pdf(396.98 KB) Additional Information: full citation, references, citings, index terms

4 A workstation-mixed model circuit simulator
Peter Odryna, Kevin Nazareth, Carl Christensen
July 1986 **Proceedings of the 23rd ACM/IEEE conference on Design automation**
Publisher: IEEE Press
Full text available: pdf(807.08 KB) Additional Information: full citation, abstract, references, citings, index terms

A new mixed mode simulator is described, which combines a behavioral timing simulator, a switch level simulator, and a new circuit-level simulator based upon the ADEPT timing simulation algorithm. These simulation algorithms are combined into a single, consistent, interactive MOS simulator. In addition, STAFAN fault simulation is provided at the transistor level to grade vectors to be used in the testing phase of design. In this paper, each algorithm is described as well as the interfacing ...

5 Incremental circuit simulation using waveform relaxation
Y.-C. Ju, R. A. Saleh
July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**
Publisher: IEEE Computer Society Press
Full text available: pdf(456.22 KB) Additional Information: full citation, references, index terms

6 An efficient non-quasi-static diode model for circuit simulation
Andrew T. Yang, Yu Liu, Jack T. Yao, R. R. Daniels
July 1993 **Proceedings of the 30th international conference on Design automation**
Publisher: ACM Press
Full text available: pdf(670.13 KB) Additional Information: full citation, references, index terms

7 An evaluation of the Chandy-Misra-Bryant algorithm for digital logic simulation
Larry Soulé, Anoop Gupta
October 1991 **ACM Transactions on Modeling and Computer Simulation (TOMACS)**, Volume 1 Issue 4
Publisher: ACM Press
Full text available: pdf(2.64 MB) Additional Information: full citation, abstract, references, citings, index terms

We explore the suitability of the Chandy-Misra-Bryant (CMB) algorithm for the domain of digital logic simulation. Our evaluation is based on results for six realistic benchmark circuits, one of them being the R6000 microprocessor form MIPS. A quantitative evaluation of the concurrency exhibited by the CMB algorithm shows that an average of 42-196 element activations can be evaluated in parallel if arbitrarily many processors are available. One major factor limiting the parallel performance ...

8 A high speed and low power SOL inverter using active body-bias
Joonho Gil, Minkyu Je, Jongho Lee, Hyungcheol Shin
August 1998 **Proceedings of the 1998 international symposium on Low power electronics and design**
Publisher: ACM Press
Full text available: pdf(506.64 KB) Additional Information: full citation, abstract, references, citings, index terms

We propose a new high speed and low power SOI inverter that can operate with efficient body-bias control and free supply voltage. The performance of the proposed circuit is

evaluated by both the BSIM3SOI circuit simulator and the ATLAS device simulator, and then compared with other reported SOI circuits. The proposed circuit is shown to have excellent characteristics. At the supply voltage of 1.5V, the proposed circuit operates 27% faster than the conventional SOI circuit with the same powe ...

9 Parallel timing simulation on a distributed memory multiprocessor

Chih-Po Wen, Katherine A. Yelick

November 1993 **Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society Press

Full text available: pdf(652.49 KB) Additional Information: full citation, references, citings

10 Parallel logic simulation of VLSI systems

Mary L. Bailey, Jack V. Briner, Roger D. Chamberlain

September 1994 **ACM Computing Surveys (CSUR)**, Volume 26 Issue 3

Publisher: ACM Press

Full text available: pdf(3.74 MB) Additional Information: full citation, abstract, references, citings, index terms

Fast, efficient logic simulators are an essential tool in modern VLSI system design. Logic simulation is used extensively for design verification prior to fabrication, and as VLSI systems grow in size, the execution time required by simulation is becoming more and more significant. Faster logic simulators will have an appreciable economic impact, speeding time to market while ensuring more thorough system design testing. One approach to this problem is to utilize parallel processing, taking ...

Keywords: circuit structure, parallel architecture, parallelism, partitioning, synchronization algorithm, timing granularity

11 Interconnect extraction: CHIME: coupled hierarchical inductance model evaluation

Satrajit Gupta, Lawrence T. Pileggi

June 2004 **Proceedings of the 41st annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(167.77 KB) Additional Information: full citation, abstract, references, index terms

Modeling inductive effects accurately and efficiently is a critical necessity for design verification of high performance integrated systems. While several techniques have been suggested to address this problem, they are mostly based on sparsification schemes for the L or L-inverse matrix. In this paper, we introduce CHIME, a methodology for non-local inductance modeling and simulation. CHIME is based on a hierarchical model of inductance that accounts for all inductive couplings at a linear cos ...

Keywords: circuit simulation, inductance modeling

12 Using Ada as a language for a CAD tool development: lessons and experiences

Jamal Guennouni

July 1988 **Proceedings of the fifth Washington Ada symposium on Ada**

Publisher: ACM Press

Full text available: pdf(1.25 MB) Additional Information: full citation, references, index terms

13. SEAMS: simulation environment for VHDL-AMS
Peter Frey, Kathiresan Nellayappan, Vasudevan Sahnmugasundaram, Ramesh Sankaran Mayiladuthurai, Chetput L. Chandrashekar, Harold W. Carter
December 1998 **Proceedings of the 30th conference on Winter simulation**
Publisher: IEEE Computer Society Press
Full text available: pdf(76.72 KB) Additional Information: full citation, references, citings, index terms

14 Parallel mixed-technology simulation
Peter Frey, Radharamanan Radhakrishnan
May 2000 **Proceedings of the fourteenth workshop on Parallel and distributed simulation**
Publisher: IEEE Computer Society
Full text available: pdf(775.49 KB) Additional Information: full citation, abstract, references, citings, index terms

Circuit simulation has proven to be one of the most important computer aided design (CAD) methods for the analysis and validation of integrated circuit designs. A popular approach to describing circuits for simulation purposes is to use a hardware description language such as VHDL. Similar efforts have also been carried out in the analog domain that has led to tools such as SPICE. However, with the growing trend of hardware designs that contain both analog and digital components, de ...

15 Miscellaneous I: Updateable simulation of communication networks
Steve L. Ferenci, Richard M. Fujimoto, Mostafa H. Ammar, Kalyan Perumalla, George F. Riley
May 2002 **Proceedings of the sixteenth workshop on Parallel and distributed simulation**
Publisher: IEEE Computer Society
Full text available: pdf(823.22 KB) Publisher Site Additional Information: full citation, abstract, references, citings

A technique called updateable simulations is proposed to reduce the time to complete multiple executions of a discrete event simulation program. This technique updates the results of a prior simulation run rather than re-execute the entire simulation to take into account variations in the underlying simulation model. A framework for creating updateable simulations is presented. This framework is applied to the problem of simulating a set of cascaded ATM multiplexers and a network of ATM switches ...

Keywords: event composition, event reuse, incremental simulation, shared computation

16 THE TRANSFER OF UNIVERSITY SOFTWARE FOR INDUSTRY USE
Rossane Wyleczuk, Lynn Meyer, Gigi Babcock
June 1983 **Proceedings of the 20th conference on Design automation**
Publisher: IEEE Press
Full text available: pdf(595.38 KB) Additional Information: full citation, abstract, references, index terms

Computer-aided engineering software is generated in abundance in educational institutions. As a major source of design automation software, universities have a lot to offer: a progressive research environment; a seemingly inexhaustible supply of software engineers in the form of undergraduates, graduate engineers, and professors; and a no-risk, multi-disciplinary design lab for experimentation. For these reasons, university software is being widely sought for use in production/commercial en ...

17 Modeling methodology: Abstract modeling for engineering and engagement level

simulations
Robert M. McGraw, Richard A. MacDonald
December 2000 **Proceedings of the 32nd conference on Winter simulation**
Publisher: Society for Computer Simulation International
Full text available: pdf(384.86 KB) Additional Information: full citation, abstract, references, citings

Today's industrial and defense communities are increasingly reliant on the use simulation to reduce cost. At times, due to their stove-piped nature, these simulations themselves have resulted in a waste of both time and money with regard to future simulation development. Current trends address this problem by promoting the development of simulation infrastructures that are scalable, portable, and interoperable over a variety of paradigms. These infrastructures, such as HLA and SPEEDES, address c ...

18 Military applications: Weapon and communication systems: simulating crisis communications
William S. Murphy, Mark A. Flournoy
December 2002 **Proceedings of the 34th conference on Winter simulation: exploring new frontiers**
Publisher: Winter Simulation Conference
Full text available: pdf(188.04 KB) Additional Information: full citation, abstract, references

This paper addresses the need for simulation of voice and data communication demands during civil and military crisis events. Modeling of federal, state, and local civilian agencies in addition to military forces can lead to better planning and execution decisions during the crisis. The need has become particularly acute following recent terrorists attacks on the United States. Preliminary crisis communication modeling capabilities exist in the Network Warfare Simulation (NETWARS) software th ...

19 Improving cache performance with balanced tag and data paths
Jih-Kwon Peir, Windsor W. Hsu, Honesty Young, Shauchi Ong
September 1996 **ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proceedings of the seventh international conference on Architectural support for programming languages and operating systems ASPLOS-VII**, Volume 31 , 30 Issue 9 , 5
Publisher: ACM Press
Full text available: pdf(1.07 MB) Additional Information: full citation, abstract, references, citings, index terms

There are two concurrent paths in a typical cache access --- one through the data array and the other through the tag array. The path through the data array drives the selected set out of the array. The path through the tag array determines cache hit/miss and, for set-associative caches, selects the appropriate line from within the selected set. In both direct-mapped and set-associative caches, the path through the tag array is significantly longer than that through the data array. In this paper ...

20 Netman: a learning network traffic controller
Bernard Silver
June 1990 **Proceedings of the 3rd international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 2 IEA/AIE '90**
Publisher: ACM Press
Full text available: pdf(963.64 KB) Additional Information: full citation, abstract, references, index terms

One of the goals of Machine Learning is the production of software that can improve itself. Such software can learn from experience and adapt to changing situations and requirements. In addition, such software can refine its knowledge-base, perhaps leading to a level of expertise beyond that of human experts. This paper describes NETMAN, a

knowledge-based program that uses a machine learning technique, Knowledge-based Learning, in the domain of Network Traffic Co ...

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